

## CLAIMS

1 1. Apparatus for enhancing debug capability in a multiprocessor circuit, comprising:  
2 a plurality of processors arranged so that data advances from processor to processor during  
3 normal operation;  
4 an advancement circuit, the advancement circuit enabling advancement of data among the  
5 processors in the event of failure of a processor; and  
6 a data bypass circuit to pass the data past a failed one of the processors.

1 2. The apparatus as in claim 1, wherein said data bypass circuit further comprises:  
2 a bypass register.

1 3. The apparatus as in claim 1, further comprising:  
2 said plurality of processors arranged to process data as a pipeline.

1 4. The apparatus as in claim 1, further comprising:  
2 said plurality of processors arranged to process data as a pipeline; and  
3 a bypass register, said bypass register having a bit location for each processor of the  
4 pipeline, each bit location capable of storing an override signal.

1 5. The apparatus as in claim 1, further comprising:

2 a memory, said memory storing computer code, said computer code having a code entry  
3 point selected by said data bypass circuit to enable a downstream processor to do the work of a  
4 failed processor.

1 6. A method for enhancing debug capability in a multiprocessor circuit, comprising:

2 advancing data among a plurality of processors, the plurality of processors arranged so that  
3 data advances from processor to processor during normal operation;

4 advancing data among the processors by an advancement circuit, in the event of failure of a  
5 processor; and

6 passing the data past a failed one of the processors by a data bypass circuit.

1 7. The method apparatus as in claim 6, further comprising:

2 indicating that a processor is to be bypassed by a bypass register.

1 8. The method as in claim 6, further comprising:

2 arranging said plurality of processors to process data as a pipeline.

1 9. The method as in claim 6, further comprising:

2 arranging said plurality of processors to process data as a pipeline; and

3 storing an override signal in a bit location of a bypass register.

1 10. The method as in claim 6, further comprising:

2 storing computer code in a memory, said computer code having a code entry point selected

3 by said data bypass circuit to enable a downstream processor to do the work of a failed processor.

1 11. Apparatus for enhancing debug capability in a multiprocessor circuit, comprising:

2 means for advancing data among a plurality of processors, the plurality of processors

3 arranged so that data advances from processor to processor during normal operation;

4 means for advancing data among the processors by an advancement circuit, in the event of  
5 failure of a processor; and

6 means for passing the data past a failed one of the processors by a data bypass circuit.

1 12. The apparatus as in claim 11, further comprising:

2 means for indicating that a processor is to be bypassed by a bypass register.

1 13. The apparatus as in claim 11, further comprising:

2 means for arranging said plurality of processors to process data as a pipeline.

1 14. The apparatus as in claim 11, further comprising:

2 means for arranging said plurality of processors to process data as a pipeline; and

3 storing an override signal in a bit location of a bypass register.

1 15. The apparatus as in claim 11, further comprising:

2 means for storing computer code in a memory, said computer code having a code entry

3 point selected by said data bypass circuit to enable a downstream processor to do the work of a

4 failed processor.

1 16. A computer readable media, comprising:

2 said computer readable media having instructions written thereon for execution on a

3 processor for the practice of the method of claim 6.

1 17. Electromagnetic signals propagating on a computer network, comprising:

2 said electromagnetic signals carrying instructions for execution on a processor for the

3 practice of the method of claim 6.